Digital implementation of a BIST method based on binary observations

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Abstract—**This article deals with a Built-in Self-Test method using only a one-bit ADC and a one-bit DAC, for use in a context of MEMS and microelectronics. It is theoretically possible to use a binary white noise and binary observations to estimate the impulse response and the output of a linear system, provided this system has good mixing properties. We show how this can be easily implemented on digital targets. The FPGA-based identification of the impulse response of a bandpass filter is performed and the experimental results are presented.**

I. INTRODUCTION

One of the major issues when designing micro electromechanical systems (MEMS) is possible dispersions due to variations in the manufacturing process, environmental variations (pressure, temperature), ageing. The MEMS behavior can differ drastically from what is expected. In order to achieve optimal performances, there is a need for devices with self-test and self-adjustment capacities [1][2]. This article focuses on a real time algorithm that can be used to identify the impulse response of a MEMS device. As opposed to existing identification methods [3], the proposed approach does not require high resolution analog to digital converters. These issues are addressed in [4] where the Basic Identification Method using Binary Observations (BIMBO) is presented. In its simplest version, BIMBO is an iterative off-line algorithm, whose performances depend on the quality of the guess of the initial model parameters. An initialization method for the BIMBO algorithm that addresses this issue is presented in [5]. This initialization method, which relies on the estimation of the covariance of the system's binary inputs and outputs, can be deployed in real time and used as a standalone identification method. This paper describes improvements of the approach presented in [5] that are suitable for its hardware implementation on a digital target (FPGA, DSP). In the first part of the paper, the principle of the algorithm is presented. Then, its digital implementation is described. The corresponding architecture is based on multiplexing: as a consequence, the number of equivalent ASIC gates is minimized, but the execution speed is reduced. In the last part, some practical examples are given to illustrate the efficiency of the approach.

II. BACKGROUND

A. Framework

Let us make the assumption that the MEMS under test can be modeled as an LTI system and that it can be described by the first n_h coefficients of its impulse response $(h_0,\ldots,h_{n_h-1})$. The method presented in [1] can be used to identify these coefficients based on the knowledge of the system input u_k and of the sign s_k of the system output y_k (Fig. 1). The input signal may either be a binary or Gaussian white noise. This paper deals with binary white noise for two reasons. First, a binary white noise is easier to generate than a Gaussian one since the implementation of a binary white noise generator only requires one linear feedback shift register (LFSR). The other reason is that the conversion from digital to analog of a binary signal is less costly (in terms of silicon area) than that of a Gaussian signal.

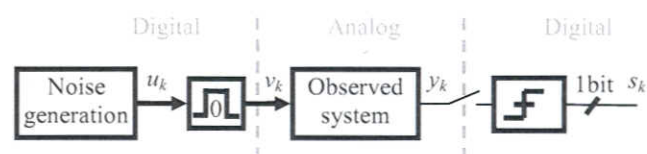


Figure 1. Experimental setup and notations, $u_k \in \{0,1\}$, $v_k \in \{-1,1\}$, $s_k \in \{0,1\}$

Notice that, due to the 1-bit ADC, there is a loss of amplitude information: multiplying the gain of the unknown system by any positive constant does not affect s_k. In order to identify the gain of the system, one would have to add an amplitude reference (such as an offset or a dithering signal) at the input of the comparator. However, in the scope of this article, we concentrate on the simpler situation represented in Fig. 1: as a consequence, only the relative amplitude of the coefficients of the impulse response will be identified.

B. Principle of the proposed approach

Under the following 2 conditions:

- u_k is a binary white noise,
- the impulse response of the tested system does not vanish quickly or, in other words, the tested system has good mixing properties,

an estimation of the p[th] coefficient of the impulse response is given by [5]:

$$\hat{h}_p = G\frac{\mathrm{erf}^{-1}\left(-2J_k(p)\right)}{\sqrt{1+2\left(\mathrm{erf}^{-1}\left(-2J_k(p)\right)\right)^2}}, \quad (1)$$

where erf^{-1} is the inverse error function and $J_k(p)$ is given by:

$$J_k(p) = \frac{1}{k+1}\sum_{l=0}^{k}\left(u_{l-p} - s_l\right)^2, \quad (2)$$

and G is a positive coefficient that can be chosen once and for all. For the sake of simplicity, we choose $G=1$. Note that $J_k(p)$ may also be written:

$$J_k(p) = \frac{1}{2}\left(1 - C_{su}(p)\right), \quad (3)$$

where $C_{su}(p)$ is an empirical estimate of the cross-covariance of s_k and u_k [5]. It is then possible to construct an "estimate" $\hat{y}_k$ (bearing in mind that some amplitude information was lost) of the system output using:

$$\hat{y}_k = \sum_{p=0}^{n_h}\hat{h}_p v_{k-p}. \quad (4)$$

At each sample time, the identification process is then divided in five steps:

A. generation of a noise sample u_k,
B. acquisition of the observed binary output signal,
C. estimation of $J_k(p)$, $0 \le p < n_h$
D. estimation of the impulse response,
E. reconstruction of the system output.

In section III, we describe a practical implementation of this approach.

III. ARCHITECTURE

In the next five sub-sections, we present a hardware architecture that implements the above-mentioned steps with a very moderate cost.

A. Noise generation

In order to generate 1-bit white noise signal, a Galois Linear Feedback Shift Register (LFSR) of order 32 has been implemented (Fig. 2) [6]

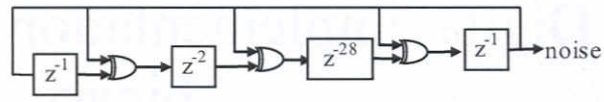


Figure 2. .Noise generator structure

B. Acquisition of binary outputs

In order to identify the coefficients of the impulse response, the last n_h values of u_k must be stored: this is accomplished by using a n_h-long delay line. As for the binary output of the system, only its current value s_k must be stored, as long as J_k is estimated iteratively, as described in sub-section C.

C. Estimation of J_k

Since u_k and s_k take only binary values 0 and 1, J_k may be written:

$$J_k(p) = \frac{1}{k+1}\sum_{l=0}^{k}\mathrm{XOR}\left(s_l, u_{l-p}\right), \quad (5$$

or as a recurrence relation:

$$J_k(p) = \frac{\mathrm{XOR}\left(s_k, u_{k-p}\right) + kJ_{k-1}(p)}{k+1}. \quad (6)$$

A possible physical implementation of (6) is shown in Fig.3. However, this solution requires a division by an integer. Moreover, this integer goes to infinity as the number of observations increases: as a consequence, the solution presented in Fig. 3 is unpractical.

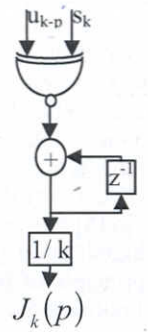


Figure 3. Exact calculation of J_k

Looking at $J_k(p)$ as the average value of $\mathrm{XOR}\left(s_l, u_{l-p}\right)$ over the last k samples, it is simple to see that expression (7) and the corresponding recurrence relation (8) will give a good approximation of $J_k(p)$ when integer b and the number of samples are large:

$$J'_k(p)=\frac{1}{b}\sum_{l=0}^{k}\left(1-\frac{1}{b}\right)^{k-l}\mathrm{XOR}\left(u_{l-p},s_l\right) \tag{7}$$

$$J'_k(p)=\frac{\mathrm{XOR}\left(u_{k-p},s_k\right)+(b-1)J'_{k-1}(p)}{b}, \tag{8}$$

In (7-8), b acts as a forgetting factor: as the value of b decreases, the weight of new observations increases and $J'_k(p)$ gives a poorer approximation of $J_k(p)$. b can be chosen to be a power of two so that the division in (8) becomes a simple shift operation. The physical implementation of equation (8) is shown in Fig. 4. Notice that no complex logic is now needed to estimate $J_k(p)$.

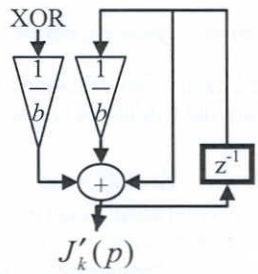


Figure 4. Approximate calculation of J_k

D. Estimation of the impulse response

In order to compute the coefficients of the impulse response from J'_k, equation (1) must be used. Since J'_k is bounded, a look-up table (LUT) can be used to evaluate the right-hand side of (1). The LUT coefficients are stored in a ROM which is addressed by the cost function.

E. Reconstruction of the system output

The "estimate" $\hat{y}_k$ of the system output can then be computed by convolution of the estimated impulse response with the system inputs. This can be done with the hardware implementation depicted in Fig. 5. The multiplication blocks appearing in Fig. 4 are in fact logic OR gates since u_k is a binary signal.

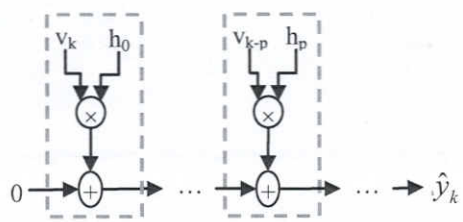


Figure 5. Calculation of $\hat{y}_k$

F. Global architecture

The real-time hardware architecture is shown in Fig. 6. Notice that the output signal $\hat{y}_k$ and impulse response coefficients are at each sample time updated by new observations. This architecture has been described in VHDL and implemented into a Xilinx Virtex 2v6000 FPGA. The whole system occupies less than 160k equivalent ASIC gates to estimate 100 impulse response coefficients. The maximum sampling frequency is about 10 MHz.

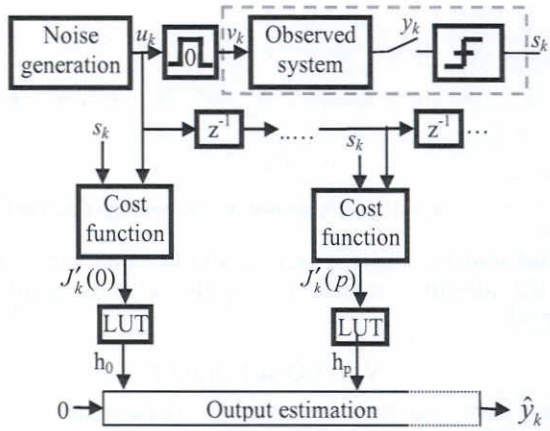


Figure 6. Global architecture

IV. Tests – Example

The algorithm has been tested on a universal active filter (UAF) [7] represented in Fig. 7. The sampling frequency is 15 kHz. The nominal values of the quality factor Q and of the natural frequency f_0 can be calculated analytically. For the values of the resistances given in Fig. 7, we find Q=1.2 and f_0=730 Hz. However, one might expect some discrepancies between these values and the actual ones, because of physical dispersions.

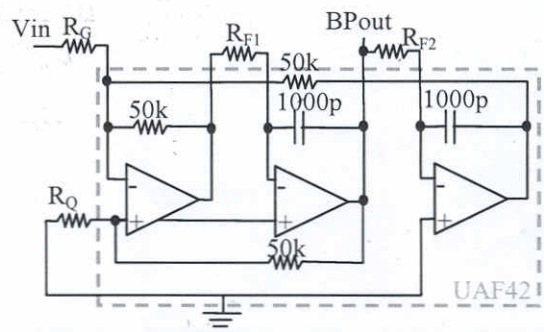
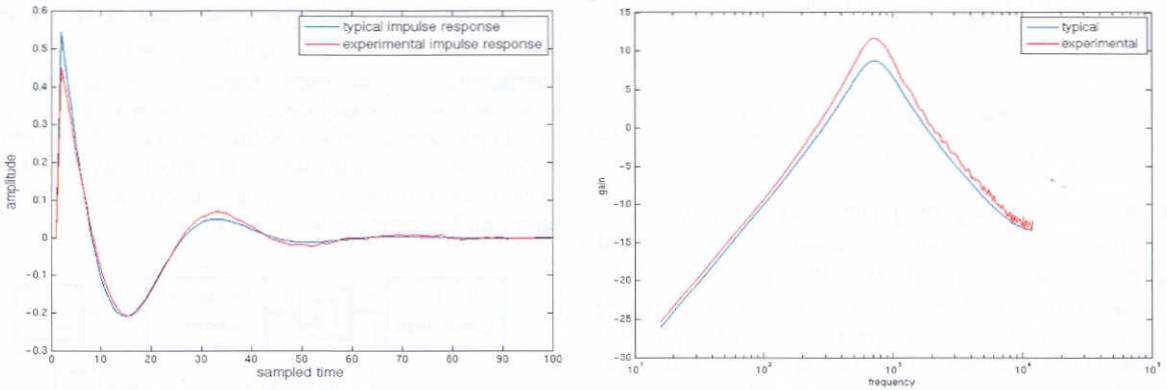


Figure 7. . Bandpass configuration of a UAF. RF1=RF2=220kΩ; RG=22kΩ; RQ=10kΩ

These discrepancies are confirmed by a test of the circuit, using the hardware architecture described in section III. The first 100 coefficients of the impulse response are identified and the results obtained after 40000 samples of the output have been processed are shown in Fig. 8 and compared to the



(a) (b)

Figure 8. Comparison between nominal (blue) and experimental results (red): (a) impulse response, (b) transfer function

nominal impulse response and transfer function. One can see that the identified system is slightly more resonant than expected.

V. CONCLUSION

We have presented a hardware implementation of the online BIST method introduced in [5], for estimating the impulse response of an unknown linear system. The only analog components required in this approach are a one-bit DAC and a one-bit ADC. We have shown how the fact that the inputs and outputs of the system are binary can be put to good use in the hardware implementation of the approach and the corresponding architecture can easily be implemented on an FPGA target, as shown in section III. A universal active filter was used to illustrate the performances of the proposed approach. Convergence acceleration procedures for the presented method and identification of infinite impulse response models are the subject of ongoing work.

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